	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1170	vertical near (FET or "field effect transistor")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 08:59
2	BRS	L2	62954	(RIE or ECR or "reactive ion etching" or "electron cyclotron resonance")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:00
3	BRS	L3	3502124	(trench or trenches or opening or groove)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01
4	BRS	L4	291735	implant$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01
5	BRS	L5	335743	dop$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	164	1 and 2 and 3 and 4 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01
7	BRS	L7	163	6 and ((@ad<"20030718") or (@rlad<"20030718"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:32
8	IS&R	L8	8	(("6356059") or ("5610085") or ("5231037") or ("5262296")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:33

DOCUMENT-IDENTIFIER: US 20020139992 A1

TITLE: Silicon carbide semiconductor device and method of fabricating the same

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Abstract Paragraph - ABTX (1):

Openings are formed in a laminate of a polycrystalline silicon film and an LTO film on a channel layer. While the laminate is used as a mask, impurities are implanted into a place in the channel layer which is assigned to a source region. Also, impurities are implanted into another place in the channel layer which is assigned to a portion of a second gate region. A portion of the polycrystalline silicon film which extends from the related opening is thermally oxidated. The LTO film and the oxidated portion of the polycrystalline silicon film are removed. While a remaining portion of the polycrystalline silicon film is used as a mask, impurities are implanted into a place in the channel layer which is assigned to the second gate region. Accordingly, the source region and the second gate region are formed on a self-alignment basis which suppresses a variation in channel length.

Application Filing Date - APD (1):

20020328

Summary of Invention Paragraph - BSTX (5):

[0004] U.S. Pat. No. 6,117,735 corresponding to Japanese patent application publication number 11-195655 discloses a method of forming a silicon carbide vertical FET in which ion implantation is implemented while a first mask and a second mask overlapping the first mask are used. As a result of the ion implantation, a first conductivity type impurity region is defined by one end of a certain portion of the first mask. The portion of the first mask and the second mask are then removed so that a second

conductivity type
impurity region is defined by another portion of the first mask. Thus, the
first conductivity type impurity region and the second conductivity type
impurity region are formed on a self-alignment basis. In the case where a mask
including a tapered end portion is used and ion implantation is conducted with
different accelerating-field voltages, the first conductivity type region and
the second conductivity type region can be formed on a self-alignment basis
using only one mask. The threshold voltage can be adjusted by controlling the
impurity concentration of the channel region. The silicon carbide vertical FET
is of a normally-off type.

Summary of Invention Paragraph - BSTX (6):

[0005] U.S. Pat. No. 6,057,558 corresponding to Japanese patent application publication number 10-308512 discloses a trench gate type power
MOSFET including a thin film of silicon carbide which defines a side of a
trench. Specifically, the power MOSFET includes an n-type thin semiconductor
film defining a side of the trench, and a gate oxide film occupying a bottom of
the trench. The power MOSFET further includes an n.sup.--type epitaxial layer
and a p-type epitaxial layer between which an n.sup.+-type epitaxial layer
extends. The p-type epitaxial layer, the n.sup.+-type epitaxial layer, and the
n.sup.--type epitaxial layer compose a pn.sup.+n.sup.-diode. The impurity
concentration and the thickness of the n.sup.+-type epitaxial layer are chosen
so that the withstand voltage of the pn.sup.+n.sup.- diode will be lower than
the withstand voltage of a surface of the gate oxide film in the trench bottom.
As a result, the pn.sup.+n.sup.- diode undergoes avalanche breakdown before the
trench bottom does. Therefore, it is possible to prevent destruction of the
gate oxide film.

Summary of Invention Paragraph - BSTX (7):

[0006] Heinz Mitlehner et al have reported "Dynamic characteristics of high voltage 4H-SiC vertical JFETs", 1999 IEEE, pages 339-342. Specifically, Heinz Mitlehner et al fabricated fully implanted SiC VJFETs on n-type epilayers grown on the Si(0001)-face of n-type 4H-SiC substrates. The epilayers were grown in two steps. The first epilayer was formed. After registration masks were defined, the first epilayer was exposed to ion implantation so that the buried p-layer was implanted with aluminum. Then, the second epilayer creating the channel and pinch off region was grown onto the first epilayer. The p-gate region was implanted over the whole cell area. In three etching steps, the gate overlay, the source area and the short connection of the source region to the buried p-layer were defined. To avoid breakdown due to field crowding at the edges, a JTE-edge termination was used. After the wafers were annealed, a field oxide was deposited. Ni-contacts on back and front were defined via lithography and lift-off. Ater a short contact anneal, the insulation oxide was deposited and patterned via dry etching. Finally, the metallization was thermally evaporated and patterned by wet etching.

Summary of Invention Paragraph - BSTX (8):

[0007] Japanese patent application publication No. 11-274173 discloses a method of fabricating a silicon carbide semiconductor device in which a mask member is formed on an n.sup.--type silicon carbide epitaxial layer. Prescribed areas of the mask member are provided with openings which have inclined side surfaces. Ion implantations into the n.sup.--type silicon carbide epitaxial layer via the openings are performed so that p.sup.--type silicon carbide base regions and n.sup.+-type source regions are formed therein. The n.sup.+-type source regions are smaller in junction depth than the p.sup.--type silicon carbide base regions. Since only one mask is used in

this way, the formation of the p.sup.--type silicon carbide base regions and the n.sup.+-type source regions is based on self-alignment. Therefore, the positions of the p.sup.--type silicon carbide base regions and the n.sup.+-type source regions are accurate.

Summary of Invention Paragraph - BSTX (9):

[0008] Japanese patent application publication number 8-288500 discloses a silicon carbide semiconductor device including a planar-type pn junction. An edge of the planar-type pn junction is of a thin flat shape to suppress concentration of electric field. The pn junction is formed by ion implantation using a mask which is made as follows. After a process of providing close adhesion between a photoresist film and a mask film is implemented, the combination of the films is exposed to isotropic etching to form the mask.

Summary of Invention Paragraph - BSTX (13):

[0011] A first aspect of this invention provides a method of fabricating a silicon carbide semiconductor device. The method comprises the steps of forming a semiconductor layer (2) on a main surface of a semiconductor substrate (1), the semiconductor layer (2) and the semiconductor substrate (1) being of a first conductivity type, the semiconductor layer (2) being made of silicon carbide, the semiconductor substrate (1) being made of silicon carbide, the semiconductor layer (2) being higher in resistivity than the semiconductor substrate (1); forming a first gate region (3) in a surface portion of the semiconductor layer (2), the first gate region (3) being of a second conductivity type different from the first conductivity type; forming a channel layer (5) of the first conductivity type on the semiconductor layer (2) and the first gate region (3); forming a source region (6) of the first conductivity type in the channel layer (5), the source region (6) being opposed to the first

gate region (3); forming a second gate region (7) in a surface portion of the channel layer (5), the second gate region (7) being of the second conductivity type and containing a positional range opposed to the source region (6); forming a recess (8) in the channel layer (5), the recess (8) extending through the second gate region (7) and the source region (6) and reaching the first gate region (3); forming a first gate electrode (9, 33, 42), a source electrode (9, 32, 41), and a second gate electrode (10, 32, 43), the first gate electrode (9, 33, 42) being electrically connected with the first gate region (3), the source electrode (9, 32, 41) being electrically connected with the source region (6), the second gate electrode (10, 32, 43) being electrically connected with the second gate region (7); and forming a drain electrode (12) on a back surface of the semiconductor substrate (1). The step of forming the source region (6) and the step of forming the second gate region (7) comprise the sub-steps of (a) placing first and second mask films (21, 22) on the channel layer (5), the first mask film (21) being covered with the second mask film (22); (b) forming first and second openings (21A, 22A) in the first and second mask films (21, 22) respectively; (c) implanting first ions into a first predetermined place in the channel layer (5) which is assigned to the source region (6) while using the first and second mask films (21, 22) as a mask, the first ions being first impurities corresponding to the first conductivity type; (d) implanting second ions into a second predetermined place in the channel layer (5) which is different from the first predetermined place and is assigned to a portion of the second gate region (7) while using the first and second mask films (21, 22) as a mask, the second ions being second impurities corresponding to the second conductivity type; (e) oxidating a portion of the

other
words, the outer portion is smaller in junction depth than the inner portion.
The inner edge of the shallow portion (the outer portion) is a prescribed
distance away outward from the outer edge of the greatly-doped portion. Thus,
the inner edge of the shallow portion is the prescribed distance away outward
from the outer edge of the n.sup.+-type source region 6. In FIG. 2, the
left-hand horizontal distance S1 between the outer edge of the n.sup.+-type
source region 6 and the outer edge of the deep portion (the inner portion) of
the second gate region 7 is equal to the right-hand horizontal distance S2
between the outer edge of the n.sup.+-type source region 6 and the outer edge
of the deep portion of the second gate region 7.

Detail Description Paragraph - DETX (20):
[0048] An LTO (low temperature oxide) film 20 is superposed on a prescribed
area of an upper surface of the n.sup.--type epitaxial layer 2. The LTO film
20 is patterned by photolithography so that a prescribed portion of the LTO
film 20 has an opening 20A extending through the wall thereof. Ion
implantations into the n.sup.--type epitaxial layer 2 are implemented while the
LTO film 20 is used as a mask. Specifically, nitrogen ions or phosphorus ions
being impurities corresponding to the n-type conductivity are implanted via the
opening 20A into a predetermined place in the n.sup.--type epitaxial layer 2
which is assigned to an n.sup.+-type body break region 4. Subsequently, boron
ions being impurities corresponding to the p-type conductivity are implanted
via the opening 20A into a predetermined place in the n.sup.--type epitaxial
layer 2 which is assigned to a first gate region 3. At this time, aluminum
ions may be implanted via the opening 20A into a predetermined surface portion
of the n.sup.--type epitaxial layer 2 which is assigned to the first gate
region 3 for providing contact with the first gate region 3.

Detail Description Paragraph - DETX (21):

[0049] With reference to FIG. 4, after the ion implantations, implanted ions are activated. For example, the ion-implanted n.sup.--type epitaxial layer 2 is subjected to ramp anneal based on RTA (rapid thermal annealing). As a result of the ramp anneal, the first gate region 3 and the n.sup.+-type body break region 4 are formed. Boron atoms are diffused out of the first gate region 3 by the ramp anneal so that a p.sup.--type region 3a is formed. Thereafter, the LTO film 20 is removed from the n.sup.--type epitaxial layer 2.

Detail Description Paragraph - DETX (23):

[0051] With reference to FIG. 6, a polycrystalline silicon film 21 is superposed on an upper surface of the channel layer 5. An LTO film 22 is superposed on an upper surface of the polycrystalline silicon film 21. Thus, a laminate of the polycrystalline silicon film 21 and the LTO film 22 is formed on the upper surface of the channel layer 5. The LTO film 22 may be replaced by a nitride film. The polycrystalline silicon film 21 and the LTO film 22 are patterned by photolithography so that prescribed portions of the polycrystalline silicon film 21 and the LTO film 22 have openings 21A and 22A extending through the walls thereof. The openings 21A and 22A are located in places opposed to an inner area of the first gate region 3. The openings 21A and 22A are of a same shape. The openings 21A and 22A align with the first gate region 3 as viewed from the top.

Detail Description Paragraph - DETX (24):

[0052] Ion implantations into the channel layer 5 are implemented while the laminate of the polycrystalline silicon film 21 and the LTO film 22 is used as a mask. Specifically, nitrogen ions or phosphorus ions being impurities corresponding to the n-type conductivity are implanted via the openings 21A and

22A into a predetermined place 6A in the channel layer 5 which is assigned to
an n.sup.+-type source region 6. Subsequently, boron ions or aluminum ions
being impurities corresponding to the p-type conductivity are implanted via the
openings 21A and 22A into a predetermined place 7A in the channel layer 5 which
is assigned to a greatly-doped portion of a second gate region 7.

Detail Description Paragraph - DETX (25):
[0053] With reference to FIG. 7, after the ion implantations, the polycrystalline silicon film 21 is subjected to thermal oxidation (oxidization). Since the polycrystalline silicon film 21 is covered with the
LTO film 22, only a given inner portion of the polycrystalline silicon film 21
which extends outward of the opening 21A is oxidated (oxidized). The oxidated
portion of the polycrystalline silicon film 21 extends from a position
coincident with the position of a side of the opening 21A to a position a given
distance away outward from the outer edge of the predetermined place 6A or 7A.
Only a portion 21B of the polycrystalline silicon film 21 remains on the
channel layer 5 without being oxidated.

Detail Description Paragraph - DETX (26):
[0054] With reference to FIG. 8, the LTO film 22 and the oxidated portion of
the polycrystalline silicon film 21 are removed from the semiconductor body
(the semiconductor wafer) including the channel layer 5. As a result, there is
only the remaining polycrystalline silicon film 21B on the channel layer 5.
The remaining polycrystalline silicon film 21B has an opening 21D extending
through the wall thereof. During the removal of the oxidated portion of the
polycrystalline silicon film 21, the opening 21A expands into the opening 21D
on an isotropic basis while the center of the expanding opening remains fixed.
An area of the upper surface of the channel layer 5 which is uncovered from the
remaining polycrystalline silicon film 21B extends over the first gate region 3

and the n.sup.+-type body break region 4 as viewed from the top. While the remaining polycrystalline silicon film 21B is used as a mask, boron ions or aluminum ions being impurities corresponding to the p-type conductivity are implanted into the channel layer 5. A deep surface portion of the channel layer 5 which is exposed in the opening 21D undergoes ion implantation. On the other hand, a shallow surface portion of the channel layer 5 which is covered with the remaining polycrystalline silicon film 21B undergoes ion implantation. The deep surface portion of the channel layer 5 has a thickness greater than that of the shallow portion thereof. The deep surface portion and the shallow surface portion of the channel layer 5 occupy a predetermined place assigned to a second gate region 7. The deep surface portion and the shallow surface portion of the channel layer 5 correspond to the deep portion and the shallow portion (the inner portion and the outer portion) of the second gate region 7, respectively. Then, the remaining polycrystalline silicon film 21B is removed from the semiconductor body including the channel layer 5.

Detail Description Paragraph - DETX (27):

[0055] With reference to FIG. 9, after the removal of the remaining polycrystalline silicon film 21B, implanted ions are activated by heat treatment. As a result, the n.sup.+-type source region 6 and the second gate region 7 are formed. Since the formation of the n.sup.+-type source region 6 is implemented by the steps including the ion implantation via the opening 21A (see FIG. 6), the position of the n.sup.+-type source region 6 is determined by the position of the opening 21A. The oxidated portion of the polycrystalline silicon film 21 extends around the opening 21A, and the oxidated portion and the opening 21A have a common center (see FIGS. 6 and 7). As previously mentioned, the oxidated portion of the polycrystalline silicon film

21 is
removed so that the remaining polycrystalline silicon film 21B occurs (see FIG.
8). The opening 21D through the remaining polycrystalline silicon film 21B
which occurs after the removal of the oxidated portion of the polycrystalline
silicon film 21 has a center coincident with that of the opening 21A. The deep
portion (inner portion) of the second gate region 7 is formed by the steps
including the ion implantation via the opening 21D through the remaining
polycrystalline silicon film 21B. Accordingly, the position of the deep
portion of the second gate region 7 depends on the position of the opening 21A.
Thus, the formation of the n.sup.+-type source region 6 and the deep portion of
the second gate region 7 is based on self-alignment. Therefore, the left-hand
horizontal distance S1 between the outer edge of the n.sup.+-type source region
6 and the outer edge of the deep portion of the second gate region 7 is equal
to the right-hand horizontal distance S2 between the outer edge of the
n.sup.+-type source region 6 and the outer edge of the deep portion of the
second gate region 7 (see FIG. 2).

Detail Description Paragraph - DETX (28):
[0056] With reference to FIG. 10, an LTO film 23 is placed on an upper
surface of the second gate region 7. The LTO film 23 is patterned by
photolithography so that a prescribed portion of the LTO film 23 which is
opposed to the greatly-doped portion (inner portion) of the second gate region
7 has an opening 23A extending through the wall thereof.

Detail Description Paragraph - DETX (29):
[0057] With reference to FIG. 11, after the formation of the opening 23A
through the LTO film 23, the semiconductor body is subjected to etching (for
example, RIE or reactive ion etching) so that a recess 8 is formed therein.
The recess 8 extends through the second gate region 7 and the n.sup.+-type

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1170	vertical near (FET or "field effect transistor")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 08:59
2	BRS	L2	62954	(RIE or ECR or "reactive ion etching" or "electron cyclotron resonance")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:00
3	BRS	L3	3502124	(trench or trenches or opening or groove)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01
4	BRS	L4	291735	implant$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01
5	BRS	L5	335743	dop$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01

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6	BRS	L6	164	1 and 2 and 3 and 4 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:01
7	BRS	L7	163	6 and ((@ad<"20030718") or (@rlad<"20030718"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 09:32
8	IS&R	L8	8	(("6356059") or ("5610085") or ("5231037") or ("5262296")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 10:17
9	BRS	L9	115866	(second! near 3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 10:20
10	BRS	L10	33	1 and 2 and 3 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 10:20

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	16	("20020024081" | "20020058381" | "20020113263" | "20030073271" | "20040031987" | "4262296" | "4651184" | "4661832" | "5208657" | "5231037" | "5326711" | "5610085" | "6277751" | "6316807" | "6356059" | "6673681").PN.	US-PGPUB; USPAT; USOCR	2004/12/01 10:26
12	BRS	L12	0	("6818939").URPN.	USPAT	2004/12/01 10:29

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	2540	((438/242) or (438/259) or (438/270) or (438/271) or (438/272)).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:30
2	BRS	L2	1221	(vertical near (FET or "field effect transistor")) or vfet or v-fet	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:30
3	BRS	L3	3502124	(trench or trenches or opening or groove)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:31
4	BRS	L4	72	1 and 2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:54
5	IS&R	L7	1765	(438/270).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:55

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	IS&R	L8	369	(438/271).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:55
7	IS&R	L9	93	(438/272).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:55
8	IS&R	L5	166	(438/242).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:55
9	IS&R	L6	457	(438/259).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 18:00
10	IS&R	L10	369	(438/271).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 18:14

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1	IS&R	L1	2540	((438/242) or (438/259) or (438/270) or (438/271) or (438/272)).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:30
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4	BRS	L4	72	1 and 2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:54
5	IS&R	L5	166	(438/242).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 17:55

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7	IS&R	L10	369	(438/271).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 18:14
8	IS&R	L8	369	(438/271).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 18:15
9	IS&R	L9	93	(438/272).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 18:26
10	IS&R	L7	1765	(438/270).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/12/01 18:30